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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,432	09/23/2003	Bing Lu	SCI2878TP	2381
23125	7590	08/02/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			ROSASCO, STEPHEN D	
		ART UNIT	PAPER NUMBER	
		1756		

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/668,432	LU ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 23 September 2003.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 23 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>9/23/03</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**Detailed Action**

The disclosure is objected to because of the following informalities: in the abstract line 5, "which is can be".

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Mangat et al. (6,653,053) or Levinson et al. (6,872,497) or Chan (6,908,716).

The claimed invention is directed to a bilayer hardmask used to manufacture a mask, which can be implemented to pattern a resist on a semiconductor wafer. The bilayer hardmask can have two layers: a first hardmask layer 28 and a second hardmask layer 30. The first hardmask layer 28 may be carbon and can be etched selective to the overlying second hardmask layer 30 and an underlying absorber structure 20. In another embodiment, the second hardmask layer 30 is a transparent layer of SiON, SiN, or SiO<sub>2</sub>. The bilayer hardmask allows for a thinner resist to be used during fabrication of the mask.

Mangat et al. teach a method of patterning a first photoresist layer on a semiconductor wafer using an attenuated phase shifting reflective mask, comprising:

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providing a mask substrate having a reflective layer; depositing an attenuating phase shift layer over the reflective layer; depositing a buffer layer over the attenuating phase shift layer; depositing a repairable layer over the buffer layer; depositing a second photoresist layer over the repairable layer; patterning the second photoresist layer to form a patterned photoresist layer; etching the repairable layer using the patterned photoresist layer as a first mask to form a patterned repairable layer; removing the patterned photoresist layer; inspecting and repairing the patterned repairable layer to form a patterned repaired layer; etching the buffer layer using the patterned repaired layer as a second mask to form a patterned buffer layer; removing the patterned repaired layer; etching the attenuating phase shift layer using the patterned buffer layer as a third mask; removing the patterned buffer layer to form the attenuated phase shifting reflective mask; applying the first photoresist to the semiconductor wafer; and reflecting radiation off the attenuated phase shifting reflective mask to the first photoresist on the semiconductor wafer to provide an exposed pattern on the photoresist.

And wherein the attenuating phase shift layer is characterized as being selectively etchable with respect to the reflective layer and comprises chromium.

And wherein the buffer layer comprises silicon oxynitride.

Levinson et al. teach a method of making a reflective lithography mask comprising: forming a reflective coating that is reflective to lithography radiation on a top surface of a substrate that is substantially absorbent to EUV lithography radiation; forming a masking material over the reflective coating; patterning the masking material so as to correspond to a desired circuit layout; inspecting the masking material for defects therein by shining a light or a beam of energetic particles at the mask, detecting an insufficient amount of

masking material where an excess amount of particles are scattered from or an excess amount of light is reflected from the reflective coating at locations that are to be covered with masking material, and detecting unwanted masking material where an insufficient amount of particles are scattered from or an insufficient amount of light is reflected from the reflective coating at locations that are not to be covered with masking material; rectifying defects found in the masking material; patterning the reflective coating so as to correspond to the desired circuit layout with the patterned masking material serving as a mask after the defects are rectified; and removing the masking material.

And wherein forming a masking material over the reflective material comprises: forming a hardmask over the reflective coating; and forming a resist over the hardmask.

And wherein the reflective coating is patterned via etching with the patterned hardmask serving as a mask.

And wherein an etchant utilized to etch the reflective coating etches the reflective coating at a rate that is faster than the etchant etches the patterned hardmask.

Chan teaches a finished photomask to be used to create an image on an image plane by means of a photolithographic process, said photomask comprising: (a) a substantially transparent substrate; (b) a patterned layer of opaque material disposed on said substantially transparent substrate; and (c) a patterned layer of hard mask material made from materials, which were selectively resistant to etching in the formation of said finished photomask to account for differences in etch rates in areas of said photomask having larger portions of said pattern layer of opaque material removed than other areas of said photomask, and disposed on said layer of opaque material, wherein substantially the same pattern is formed in said opaque material as is formed in said hard mask material, and said

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patterns correspond to a scaled negative of the image to be formed on said image plane; further comprising a patterned layer of anti-reflective material disposed between said layer of opaque material and said layer of hard mask material.

And wherein said hard mask material is between 50 and 500 ANG thick and is comprised of Sisub3 Nsub4 or SiOsub2.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



S. Rosasco  
Primary Examiner  
Art Unit 1756

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07/25/05